THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 9

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte KELVIN D. NILSEN

_____

Appeal No.1997-3240
Application 08/176,940[1]

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ON BRIEF

_____

Before THOMAS, KRASS and FLEMING, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the rejection of claims 1 through 4, 8, 9 and 13 through 17. Claims 5 through 7 and

[1] Application for patent filed January 4, 1994.

10 through 12 are objected to, for depending upon a rejected base claim.

Appellant's invention relates to an object space manager circuit in a computer that provides control over live object memories that are being used by the CPU in the performance of an application program. More specifically, Appellant, on page 4 of the specification, discloses that an encoding means generates locator codes for each word of an object and a locating means identifies the cell containing the header of an object. Appellant on pages 7 through 9, further adds that the coding means uses a hierarchial coding scheme that stores in a code memory three levels of codes for each object word stored in the memory. Thus, the header address of an object is determined from the address of any word in the object. The requirements of each coding level is further outlined to be related to the particular number of most significant bits of the word address within an object which ultimately determines the object header address.

Representative independent claim 1 is reproduced as follows:

1. An object space manager circuit comprising:

a code memory for storing a plurality of code words for a plurality of encoding levels, the addresses of the code words for each encoding level being denoted by an ordered sequence of integers beginning with 0, a 0 being stored initially at each memory address;

a means for entering simultaneously into the code memory at a plurality of addresses a code word for each of a plurality of encoding levels, the addresses for each level being those included within a specified beginning address and a specified ending address, the code words, the encoding levels, the beginning addresses, and the ending addresses being supplied through an input port.

The Examiner relies on the following reference:

McEntee et al. (McEntee) 4,797,810 Jan. 10, 1989

Claims 13 through 17 stand rejected under 35 U.S.C. § 112, second paragraph, as being single means claims having "undue breadth." Claims 1 through 4, 8 and 9 stand rejected under 35 U.S.C. § 103 over McEntee.

Rather than repeat the arguments of Appellant and the Examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

After careful review of the evidence before us, we do not agree with the Examiner that claims 13 through 17 are properly

rejected under 35 U.S.C. § 112 and that claims 1 through 4, 8 and 9 are properly rejected under 35 U.S.C. § 103. Accordingly, we reverse.

Turning to the rejection of claims 13 through 17 under 35 U.S.C. § 112, second paragraph, Appellant, on page 14 of the brief, argues that apparatus claims 13 through 17 depend from multi-step process claims 8 through 12 and have proper linking claim format. Appellant further adds that the base claims satisfy the requirements of 35 U.S.C. § 112, second paragraph, and therefore, claims 13 through 17 must satisfy those same requirements.

In response to Appellant's arguments, the Examiner, on page 4 of the answer, points out that claims 13 through 17 are unduly broad since all possible apparatuses that perform those processes have to be considered. The Examiner further adds that one [skilled] in the art cannot determine all possible apparatuses that perform the process as in Appellant's claims 13 through 17.

With regard to claim 13, we note that it depends from claim 8 and properly recites an apparatus for the practice of the process of claim 8. We agree with Appellant that to

determine the propriety of claim 13 under provisions of 35 U.S.C. § 112, we must first examine the base claim. We note that claim 8 recites "[a] process ... using a code memory for storing a plurality of code words" in the preamble, and "the step: entering simultaneously into the code memory ..." in the body of the claim.

35 U.S.C. § 112, paragraph 6 reads:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support
> thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof. [Emphasis ours.]

Our reviewing court in ***Rowe v. Dror***, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553, (Fed. Cir. 1997) has pointed out that "[t]erm appearing only in the preamble of the claim is affirmative structural limitation when the form of the claim and the language in the specification limits the claimed invention to that structure." See ***In re Paulsen***, 30 F.3d 1475, 1479, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (examining

"patent as a whole"); ***Vaupel Textilmaschinen KG v. Meccanica Euro Italia SPA***, 944 F.2d 870, 880, 20 USPQ2d 1045, 1053 (Fed. Cir. 1991) (looking to claims, specification, and drawings); ***Gerber Garment Tech., Inc. v. Lectra Sys., Inc.***, 916 F.2d 683, 689, 16 USPQ2d 1436, 1441 (Fed. C0..ir. 1990) (noting that preamble recitations provided antecedent basis for terms used in body of claim).

After a review of the entire disclosure as a whole, we find that “using a code memory for storing a plurality of code words” is pointed out on pages 6 through 8 of the specification as the first step in storing the sequenced addresses of the code words.

We further find that the code memory in the preamble sets out a relationship among the addresses of the code words and the “0" being stored initially at each memory address.

Additionally, the claim recites the step of “entering simultaneously ... a code word for each of a plurality of encoding levels.”

We find that independent base claim 8 does recite multiple process steps in a combination claim format and satisfies the requirements of 35 U.S.C. § 112. We note that

claims 9 through 12, which depend from and further limit claim 8, also have a combination claim format. Therefore, apparatus claims 13 through 17 do properly recite an apparatus for performing the multiple process steps of base claims 8 through 12 respectively. Accordingly, we reverse the rejection of claims 13 through 17 under 35 U.S.C. § 112.

With regard to the rejection of claims 1 through 4, 8, and 9 under 35 U.S.C. § 103 over McEntee, Appellant, on page 16 of the brief, argues that McEntee does not teach a means for simultaneously entering a code word at a plurality of addresses for each of a plurality of encoding levels. Appellant, on page 19 of the brief, further points out that McEntee's disclosure lacks any means that is the same as or equivalent to Appellant's structure of register arrays for different encoding levels. Additionally, Appellant, on pages 20 through 22, outlines the structure corresponding to the means for simultaneously entering of code words. Appellant adds that McEntee is merely concerned with copying an object, cell by cell, from "oldspace" to "newspace" without using register arrays for simultaneous entry of any part of the memory object at a plurality of addresses.

In response to Appellant's arguments, the Examiner on page 4 of the answer points out that the broad language of claims 1 and 8 merely includes the memory allocation scheme of McEntee except for the simultaneously entering of the code words. The Examiner further points out that Appellant did not define the different encoding levels for entering data. To modify the teachings of McEntee, the Examiner, on page 5 of the answer reasons that simultaneously entering of data is well known and common in the art and increases speed.

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." ***In re Hiniker Co.***, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). Claims will be given their broadest reasonable interpretation consistent with the specification, and limitation appearing in the specification are not to be read into the claims. ***In re Etter***, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985). Our reviewing court further states in ***In re Donaldson***, 16 F.3d 1189, 1193, 29 USPQ2d 1845, 1848 (Fed. Cir. 1994) that "[t]he plain and unambiguous meaning of paragraph six is that one construing means-plus-function language in a claim must look to the

specification and interpret that language in light of the corresponding structure, material, or acts described therein, and equivalents thereof, to the extent that the specification provides such disclosure."

Appellant, on pages 7 through 9 of the specification, teaches three encoding levels for each object word stored in the memory using object space manager (OSM) circuit 45. Appellant, on pages 7 and 8 of the specification, defines the addresses for each level as the particular bits of an object memory address. Appellant, on pages 13 and 14 of the specification, further discloses that the OSM includes register arrays 7 and 9 for level-1, register arrays 13 and 15 for level-2, and register arrays 1 and 3 for level-3 encoding. Appellant further teaches additional input/output register array segments and control circuitry for storing the code words.

After a review of the foregoing sections of the disclosure, we find that OSM circuit 45 is the corresponding structure for the "means for entering simultaneously into the code memory at a plurality of addresses" as recited in Appellant's claim 1. We further find that register arrays 1,

3, 7, 9, 13, 15 and the related input/output ports and circuitry specifically provide for the simultaneous entry of the code words at a plurality of addresses for each distinct encoding level.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc***., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996) ***citing W.L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference or shown to be common knowledge of

unquestionable demonstration. Our reviewing court requires this evidence in order to establish a ***prima facie*** case. ***In re Piasecki,*** 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984); ***In re Knapp-Monarch Co.***, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); ***In re Cofer***, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Furthermore, our reviewing court states in ***Piasecki***, 745 F.2d at 1472, 223 USPQ at 788 (Fed. Cir. 1984) the following:

> The Supreme Court in ***Graham v. John Deere Co.***, 383 U.S. 1, 148 USPQ 459 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under section 103. As adapted to ***ex parte*** procedure, ***Graham*** is interpreted as continuing to place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under section 102 and 103" [***citing In re Warner***, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967)].

After a review of the teachings of McEntee, we fail to find that the “means for entering simultaneously into the code memory at a plurality of addresses,” as recited in Appellant’s claim 1, is the same as the copying and updating the pointers to the objects of McEntee or an “equivalent” thereof. We disagree with the Examiner that the memory allocation system of McEntee either inherently or obviously provides

simultaneous storing of code words for different encoding levels. McEntee, in col. 4, lines 13 through 27 and claim 1, teaches a method and an apparatus for cell by cell copying of the active memory objects into a new memory area and updating the pointers to that object. However, we fail to find any teachings in McEntee that shows or leads us to Appellant's claimed means and method for storing the code words for a plurality of encoding levels or their equivalent. Additionally, McEntee merely transfers the objects by exact copying of each cell but is completely silent with regard to the means and the method for simultaneous storing of a specified code word through a range of registers at a plurality of addresses for different encoding levels.

Therefore, the limitation of "means for entering simultaneously into the code memory at a plurality of addresses a code word for each of a plurality of encoding levels," as recited in Appellant's claim 1, is absent in McEntee's disclosure. We note that the other independent claim 8 recites a process for simultaneous entering of code words similar to claim 1. Accordingly, we reverse the

rejection of claims 1 through 4, 8 and 9 under 35 U.S.C. § 103 over McEntee.

In view of the forgoing, the decision of the Examiner rejecting claims 13 through 17 under 35 U.S.C. § 112 and rejecting claims 1 through 4, 8 and 9 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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	)	BOARD OF PATENT
ERROL A. KRASS	)	
Administrative Patent Judge	)	APPEALS AND
	)	
	)	INTERFERENCES
	)	
MICHAEL R. FLEMING	)	
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